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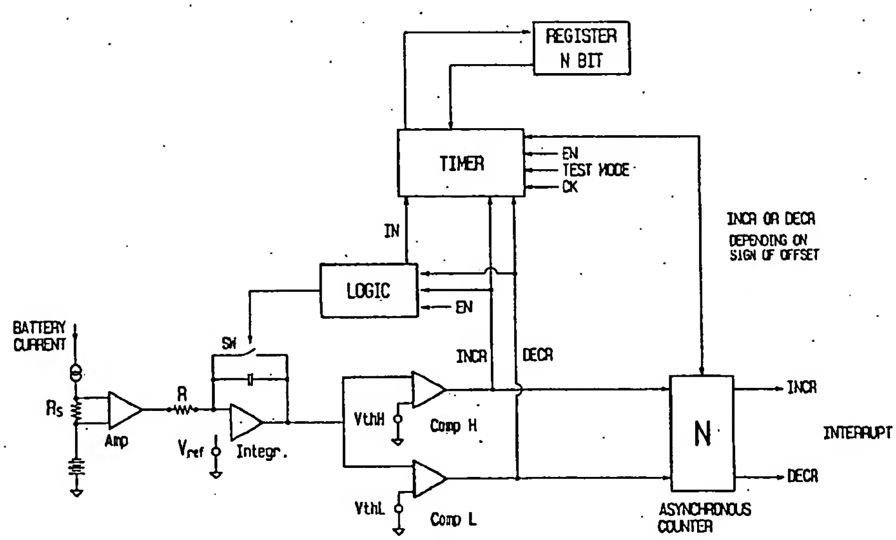
(54) **Battery charge monitor for a electronic appliance**

(57) A counter for monitoring the state of charge of the battery of an electronic apparatus comprising a current sensing circuit composed of a differential amplifier (AMP), a resettable integrator (INTEGR), a first comparator (CompH) and a second comparator (CompL) generating a logic charge interrupt signal (INCR), and a logic discharge interrupt signal (DECR), respectively, a switch (SW) for discharging the capacitance of integration (C) controlled by a logic circuit (LOGIC) at every transition of the output signal of one or the other of said first and second comparators (CompH,CompL), and processing means (N) which monitor the state of charge of the battery, further comprising a timer (TIMER) measuring the time elapsing from the start of a new integration ramp and the switching instant of either one of said first and second comparators (CompH,CompL) and a non-volatile memory register (REGISTER) containing the measure of the time interval of integration of the offset of said differential amplifier (AMP) up to the switching of either of said first and second comparators (CompH, CompL), performed during a trimming step.

The processing means (N) increments or decrements the computation of said interrupt signals (INCR, DECR) depending on the sign of the offset.



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Description

[0001] The present invention relates to systems for managing power dissipation of electronic devices powered with rechargeable batteries and in particular to indicate, for example on an LCD monitor, the state of charge of the battery.

[0002] In many familiar portable electronic apparatuses such as mobile telephones, personal computers and the like, it is important to know the charge condition of the batteries.

[0003] This function is commonly carried out by the use of a specific integrated system comprising also a charge counter (Coulomb Counter or briefly CC) which monitors the electric charge that flows in and out of battery, generating a logic interrupt signal every time a certain amount of electric charge crosses the battery, during the charge phase (charge interrupt INCR) as well as during the discharge phase, that is, of powering of the portable apparatus, (discharge interrupt DECR).

[0004] These interrupts are algebraically processed by the micro controller of the portable apparatus that obtains an indication of the state of charge of the battery. This information is either displayed on the screen in the form for example of an icon with different brightness grades or as a numerical indication of the percentage of charge of the battery or the like.

[0005] In order to evaluate the amount of available charge that flows through the battery commonly the battery current is monitored on a dedicated sensing resistor, connected electrically in series with the battery. The voltage drop on this resistor is amplified through a differential amplifier whose output signal is integrated through a dedicated integrator stage.

[0006] In the presence of an electric current flowing through the battery, a positive or negative ramp is produced at the output of the integrating stage, depending on the current direction (either a charge current or a discharge current).

[0007] The ramp is interrupted by the switching of one or the other of a pair of comparators, one for the positive ramp and the other for the negative ramp, which momentarily closes a discharge switch of the capacitance of integration and thereafter a new ramp begins and so forth. Therefore the switchings of the two comparators generate as many interrupt signals, of one or the other sign, that are fed to two respective counters, or to a unique counter which is incremented by a unit at each charge interrupt or decremented by a unit at every discharge interrupt or vice versa. In either case, the content of the counters or of the reversible counter indicates the state of charge of the battery.

[0008] The quest for minimizing power dissipation motivates the use of a sensing resistor of the battery current of a very small value, typically in the order of few tens of a mΩ (for example 50 to 100 mΩ).

[0009] The monitoring of the battery current is to some extent invalidated by the offset of the differential amplifier. Indeed, the amplifier offset sums itself to the voltage drop on the terminals of the sensing resistor and when the battery current is relatively low, for example less than a few tens of mΩ, the offset of the amplifier may be of the same order of the real signal. Moreover, during null battery current working conditions, the system will continue to integrate the offset and the counter, in absence of specific corrections, would be periodically increased or decreased depending on the sign of the offset thus providing the micro-controller with spurious information.

[0010] In order to avoid this conspicuous error a minimum current level is usually established, below which the monitoring of the current is inhibited, thus creating, in practice, a so-called dead zone, typically in the order of few mA. When the signal level is lower than a certain threshold corresponding to such a set minimum current level of the dead zone, the output signal of the amplifier in not integrated, thus averting the generation of interrupt under conditions that would be in any case grossly affected by the offset.

[0011] It is quite difficult to precisely define the limits of this dead zone and the computational error of the charge state is rather relevant.

[0012] Confronted with these difficulties and limitations of the known technique, it has now been found a charge counter that allows, according to preferred embodiment, a substantially complete compensation of the offset by carrying out a trimming step of the system or, according to an alternative embodiment, to implement a counter in which the limits of an appropriate dead zone may be accurately defined by carrying out a trimming step.

[0013] Substantially, the system of the invention is based on the use of a timer that measures the time interval between the start instant of an integration ramp of the output signal of the differential amplifier that monitors the current through the battery and the switching of one or the other comparator, and of a nonvolatile memory register where to permanently store the time interval relative to the integration of the offset established during a trimming step, done by short-circuiting the inputs of the differential amplifier that monitors the current battery. Of course, also the offset direction is permanently stored in the memory register by way of a sign bit.

[0014] According to a preferred embodiment of the Invention, during a null battery current phase, the system continues to integrate the amplifier offset causing the switching of the relative comparator which, if not compensated for, would unduly increment the relative interrupt counter. However, at the expire of the pre-established time interval, the value of which is permanently stored in the register during a trimming step, the relative interrupt counter is decremented by a unit, thus nullifying the increment due a continued integration of the offset. In presence of a battery current, the offset is integrated together with the signal present on the sensing resistor terminals, and also in these conditions, when

the pre-established and permanently stored time interval lapses, the system decrements the relative interrupt counter by a unit, thus thoroughly compensating any offset effect in computing the interrupts under any current absorption condition.

[0015] If desired, the system of the invention may also be used to implement an interrupt counter with a dead zone, the extent of which may be defined according to the real offset conditions with a high accuracy.

[0016] Assuming to be wishing to set a dead zone comprised between ±15mA, during a dedicated trimming step, a current of 15mA is forced through the sensing resistor. The timer measures the time interval (dead zone time) elapsing from the beginning of the integration and the eventual switching of the relative comparator. This information is permanently stored in the nonvolatile memory register.

[0017] During the normal functioning of the apparatus, the timer, at the beginning of each new integration phase counts backward starting from the dead zone limit time.

[0018] Therefore, if the battery current is within the dead zone range, the integration time will be greater (or at the most equal to) than the dead zone limit time and the result of the counting will be null, thus impeding an increment of the relative interrupt counter.

[0019] If the battery current is greater than the dead zone limit current, the integration time needed to trigger the relative interrupt counter will be less than the dead zone limit time and the result of the counting will be different from zero. Therefore, the interrupt counter will be correctly increased or decreased upon the switching of the relative comparator.

[0020] The attached figure shows a basic diagram of the counter of the invention.

[0021] By referring to the figure, the counter of the invention for determining the state of charge of a battery, comprises a conventional sensing circuit of the charge and discharge current of the battery. The summing circuit is composed of a differential amplifier AMP whose inputs are coupled to the terminals of a sensing resistor Rs of the battery current, and of an integrator stage INTEGR, resettable by a switch SW, that integrates the signal output by the amplifier AMP. A first comparator CompH compares the ramp output by the integrator with a first threshold VthH, eventually generating a logic charge interrupt signal INCR, while a second comparator CompL compares the same signal output by the integrator with a second threshold VthL, eventually generating a logic discharge interrupt signal DECR.

[0022] The discharge switch SW of the capacitance of integration C of the integrator is momentarily closed by a LOGIC circuit at each transition of the INCR or DECR output signals of either one or the other comparator.

[0023] According to a fundamental aspect of the invention, the counter further comprises a TIMER that is started by a command IN produced by said LOGIC circuit. The TIMER measures the interval elapsing between the starting instant of a new ramp of integration and the switching of one or of the other comparator of the pair of comparators CompH and CompL of the sensing circuit.

[0024] An N bit nonvolatile memory REGISTER contains the information of the time interval integration of the amplifier's offset up to switching of one or the other of the two comparators, depending on the direction (sign) of the amplifier's offset, written therein during a trimming step. The so stored information includes a sign bit that identifies the direction of the offset of the monitoring amplifier. The asynchronous counter N that computes the charge and discharge interrupt signals, INCR and DECR, increments or decrements the computation, depending on the sign of the offset, at the elapsing of each interval of integration of the amplifier's offset, in function of the data permanently stored in the REGISTER.

[0025] A trimming step is commanded by the TEST_MODE command, which also controls the short-circuiting of the inputs of the differential amplifier (SNIP) in order to check the offset.

[0026] In practice, depending on the offset data (magnitude and sign) of the differential amplifier determined during a trimming step, permanently stored in the REGISTER upon the completion of the trimming step, at the end of a time interval equivalent to the time of integration of the amplifier offset determined during the trimming step, the information currently contained in the asynchronous counter N is decremented or incremented by a unit, depending on the stored offset sign.

Claims

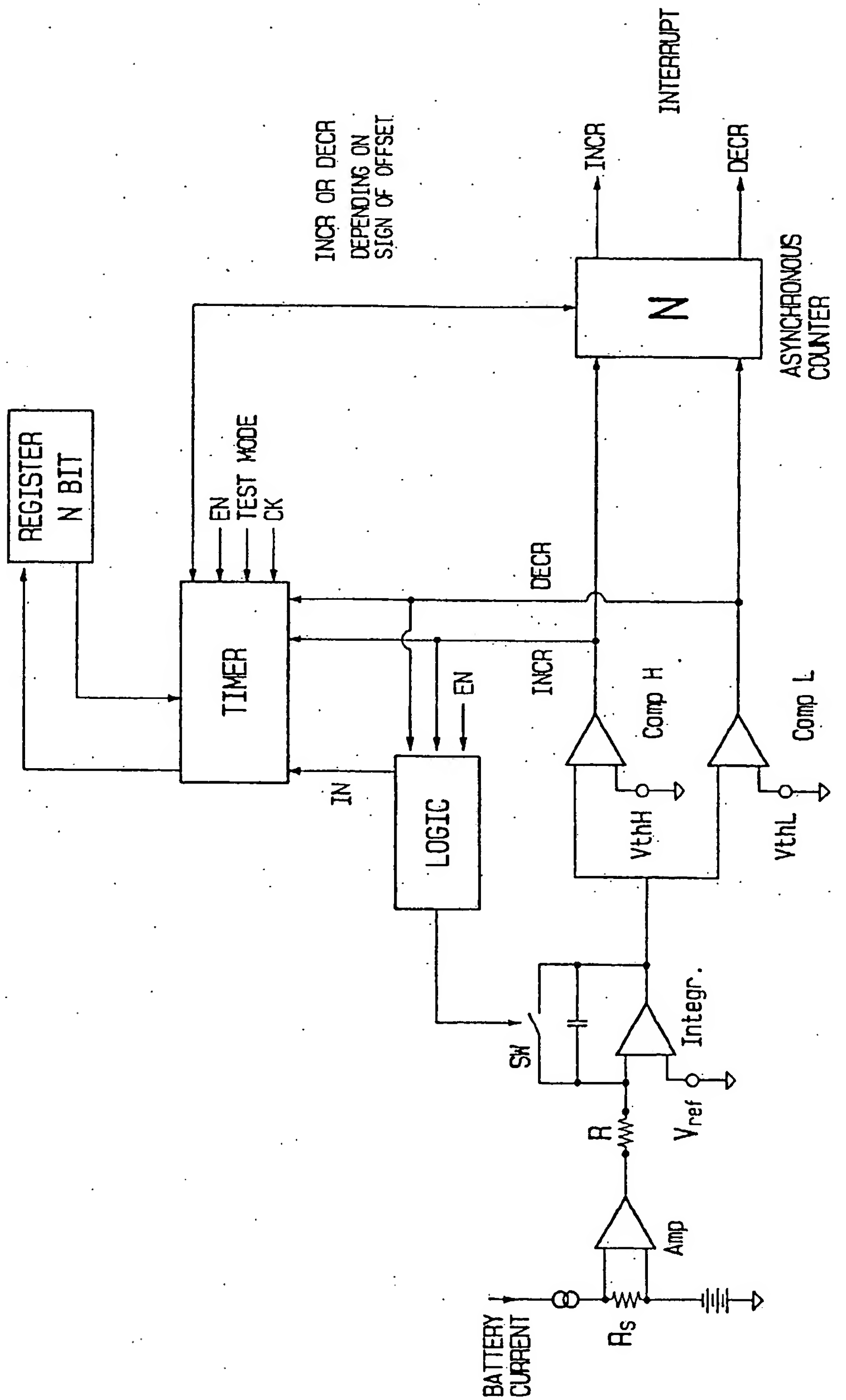
1. A charge counter for monitoring the charge of the battery state of an electronic apparatus comprising a sensing circuit of the charge and discharge current of the battery composed of a differential amplifier (AMP) having inputs coupled to the terminals of a sensing resistor (Rs) of the battery current, a resettable integrator (INTEGR) of the output signal of said amplifier (AMP), a first comparator (CompH) and a second comparator (CompL) of the output signal of said integrator generating a logic charge interrupt signal (INCR), and a logic discharge interrupt signal (DECR), respectively, a switch (SW) for discharging the capacitance of integration (C) of said integrator (INTEGR) momentarily closed by a logic circuit (LOGIC) at every transition of the output signal of one or the other of said first and second comparators (CompH, CompL), and processing means (N) of said interrupts which monitor the state of charge of the battery, characterized in that it comprises further

    a timer (TIMER) measuring the time elapsing from the start instant of a new integration ramp

and the switching instant of either one of said first and second comparators (CompH, CompL);

a nonvolatile memory register (REGISTER) containing the measure of the time interval of integration of the offset of said differential amplifier (AMP) up to the switching of either of said first and second comparators (CompH, CompL), performed by short-circuiting the inputs of said amplifier during a trimming step including a sign bit depending on which of said first or second comparator has switched;

said logic processing means (N) increments or decrements the computation of said interrupt signals (INCR, DECR) depending on the sign of the offset at the expire of each time interval of integration of the offset, permanently stored in said memory register (REGISTER).


INCR OR DECR
DEPENDING ON
SIGN OF OFFSET
INTERRUPT
INCR
DECR
N
ASYNCHRONOUS
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EUROPEAN SEARCH REPORT

Application Number
EP 99 83 0086

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION
A	GB 2 321 714 A (SAMSUNG ELECTRONICS) 5 August 1998 (1998-08-05) * abstract * * page 8, line 30 - page 9, line 27 * ---	1	G01R31/36
A	US 5 614 902 A (HOPKINS) 25 March 1997 (1997-03-25) * column 4, line 38 - line 52 * ---	1	
A	DE 41 03 470 A (SANYO ELECTRIC) 8 August 1991 (1991-08-08) * abstract; figures 1,2 * ---	1	
A	US 5 432 429 A (BENCHMARQ MICROELECTRONICS) 11 July 1995 (1995-07-11) * abstract; figures 5,6A * -----	1	
			TECHNICAL FIELDS SEARCHED
			G01R

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	19 July 1999	Iwansson, K

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ANNEX TO THE EUROPEAN SEARCH REPORT ON EUROPEAN PATENT APPLICATION NO. EP 99 83 0086

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19-07-1999

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